Docket No. 200314976-1

Amendments to the Claims:

Status of Claims:

Claims 1-24 were pending for examination.

Claims 1-11, and 14-22 are amended herein.

Claims 12, 13, 23, and 24 are cancelled herein.

Claims 1, 14, and 22 are in independent form.

1. (Currently Amended) An apparatus for producing a simulated ~~system for simulating a~~ processor performance state in a processor, comprising:

a memory ~~a data structure stored in a memory, the data structure being configured~~ to store an address of an ACPI (Advanced Configuration and Power Interface) throttling register in the processor and a set of throttling bit patterns to be selectively ~~capable of being~~ written to the ACPI throttling register, and

a logic ~~configured to receive a request to establish a desired processor performance state in a processor,~~ to select a bit pattern from the set of throttling bit patterns, and to ~~cause the processor to be throttled in a manner that simulates the desired processor performance state by writing~~ write the selected bit pattern to the ACPI throttling register to produce a simulated processor performance state without causing an actual ACPI processor performance state change.

2. (Currently Amended) The apparatus ~~system~~ of claim 1, where the memory ~~data structure is further configured~~ is to store an address of an ACPI status register from which a value related to [[a]] throttling ~~status~~ established by writing the selected bit pattern to the ACPI throttling register is to ~~can~~ be read.

3. (Currently Amended) The apparatus ~~system~~ of claim 1, where the memory is operably connected ~~connectable~~ to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions.

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4. (Currently Amended) The apparatus ~~system~~ of claim 1, the memory storing ~~where the data structure comprises~~ an ACPI table, the memory being ~~stored in a memory that is~~ operably connected ~~connectable~~ to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions.

5. (Currently Amended) The apparatus ~~system~~ of claim 1, the logic being configured to establish ~~where the data structure comprises~~ an ACPI table ~~stored~~ in a Basic Input Output System (BIOS), where to establish the table includes copying one or more values from the memory to the BIOS ~~configured to facilitate controlling one or more processor functions~~.

6. (Currently Amended) The apparatus ~~system~~ of claim 1, where the set of throttling bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state.

7. (Currently Amended) The apparatus ~~system~~ of claim 1, where the processor does not have a variable voltage supply.

8. (Currently Amended) The apparatus ~~system~~ of claim 1, where the set of throttling bit patterns facilitates simulating two or more processor performance states.

9. (Currently Amended) The apparatus ~~system~~ of claim 8, where the two or more processor performance states include eight processor performance states simulated by throttling the processor 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time.

10. (Currently Amended) The apparatus ~~system~~ of claim 1, where the ACPI throttling register is configured to cause the processor to be throttled by asserting a signal on a STOPCLK# line connected to the processor.

11. (Currently Amended) The apparatus ~~system~~ of claim [[1]]7, where the processor does not have a variable frequency clock.

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12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) A method for causing a processor to operate as though an ACPI processor performance state had been established without actually causing an ACPI processor performance state change~~simulating a processor performance state~~, comprising:

receiving a request to establish an actual processor performance state in a processor;

accessing a data structure to acquire a throttling bit pattern to write to an ACPI throttling register and an address for the ACPI throttling register; and

establishing a simulated processor performance state ~~simulating a processor performance state~~ by ~~causing the processor to be throttled in response to~~ writing the bit pattern to the ACPI throttling register.

15. (Currently Amended) The method of claim 14, including establishing the data structure as an ACPI table in a Basic Input Output System (BIOS) operably connected ~~connectable~~ to the processor.

16. (Currently Amended) The method of claim 15, where establishing the data structure includes writing a set of throttling bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table.

17. (Currently Amended) The method of claim 16[[14]], where the actual processor performance state corresponds to one of a higher performance state and a lower performance state.

18. (Currently Amended) The method of claim 16[[14]], where the actual processor performance state corresponds to one of two or more user defined processor performance states.

19. (Currently Amended) The method of claim 16[[14]], where the actual processor performance state corresponds to one of eight processor performance states including a state where the processor is throttled one of 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time.

20. (Currently Amended) The method of claim 14, where writing the throttling bit pattern to the ACPI throttling register causes a signal to be asserted on a STOPCLK# line into the processor.

21. (Currently Amended) The method of claim 14, including:

acquiring an address of an ACPI status register configured to report a value related to [[a]] throttling ~~status of~~ the processor;

reading the value from the ACPI status register; and

selectively reporting a success or error condition based on the value.

22. (Currently Amended) A computer-readable medium storing processor executable instructions that when executed by a processor cause the processor to perform a method ~~operable to perform a method for simulating a processor performance state in a processor~~, the method comprising:

establishing an ACPI table in a Basic Input Output System (BIOS) operably connected ~~connectable~~ to the processor, where establishing the ACPI table includes writing a set of throttling bit patterns to the ACPI table[[,]] and writing an address of an ACPI throttling register to the ACPI table;

receiving a request to establish an actual processor performance state in the processor, where the actual processor performance state corresponds to one of a higher frequency state and a lower frequency state;

accessing the ACPI table to acquire a throttling bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register; and

~~causing a processor to simulate a processor performance state by throttling the processor by~~ writing the bit pattern to the ACPI throttling register to cause the actual processor performance state to be simulated without actually causing an ACPI state change.

23. (Cancelled)

24. (Cancelled)